Powering up GaN MOSFETs

In the past few years a new application for nitride semiconductors has been developing for high-power radio/microwave frequency amplifiers based on high critical field and carrier mobility properties. However, the transistors that have been produced have high gate leakage, leading to severe power losses, and it is desirable to develop suitable insulated gate structures. Recently, this work has been making progress, reports Dr Mike Cooke.

For some 20 years, there has been a drive to research and develop gallium nitride and related III–N compound semiconductor materials for electronic applications. The attractive properties of GaN include a wide direct energy bandgap of 3.4eV, a large critical electric field of 3MV/cm, carrier mobility comparable to that of silicon, and good thermal conductivity.

Until recently, nitride semiconductor development has been propelled forward by the ability, in principle, to emit light in the wavelength range 590–190nm, corresponding to photon energies of 2.0–6.2eV. This spectral range covers orange, yellow, green, blue, violet and ultraviolet light, based on various mixtures of aluminium (AlN, for which the bandgap is E_g~6.2eV), gallium and indium (InN, E_g~2eV) with nitrogen.

Now, due to its critical field and carrier mobility properties, GaN is being used to produce high-power-density transistors for radio frequencies up to tens of gigahertz. The smaller size of the resulting devices enables better impedance matching and hence better signal power transmission into and out of the device. These components are being marketed for base-stations used for mobile phone to network communications (~2GHz).

So far, the GaN devices produced for power applications have been high-electron mobility transistors (HEMTs) with the gate operating through a reverse-biased Schottky junction with the semiconductor material. However, HEMTs suffer from high power losses from gate leakage and normally-on characteristics compared with components with an insulated gate, such as metal–oxide–semiconductor field effect transistors (MOSFETs). This is where silicon integrated device technology has been so successful in creating effective MOSFET structures that have been difficult to produce in other technologies. The basis for silicon MOSFETs has been the ease of growing silicon dioxide insulator on silicon with low densities of charge trap states and fixed charges near semiconductor–insulator interfaces.

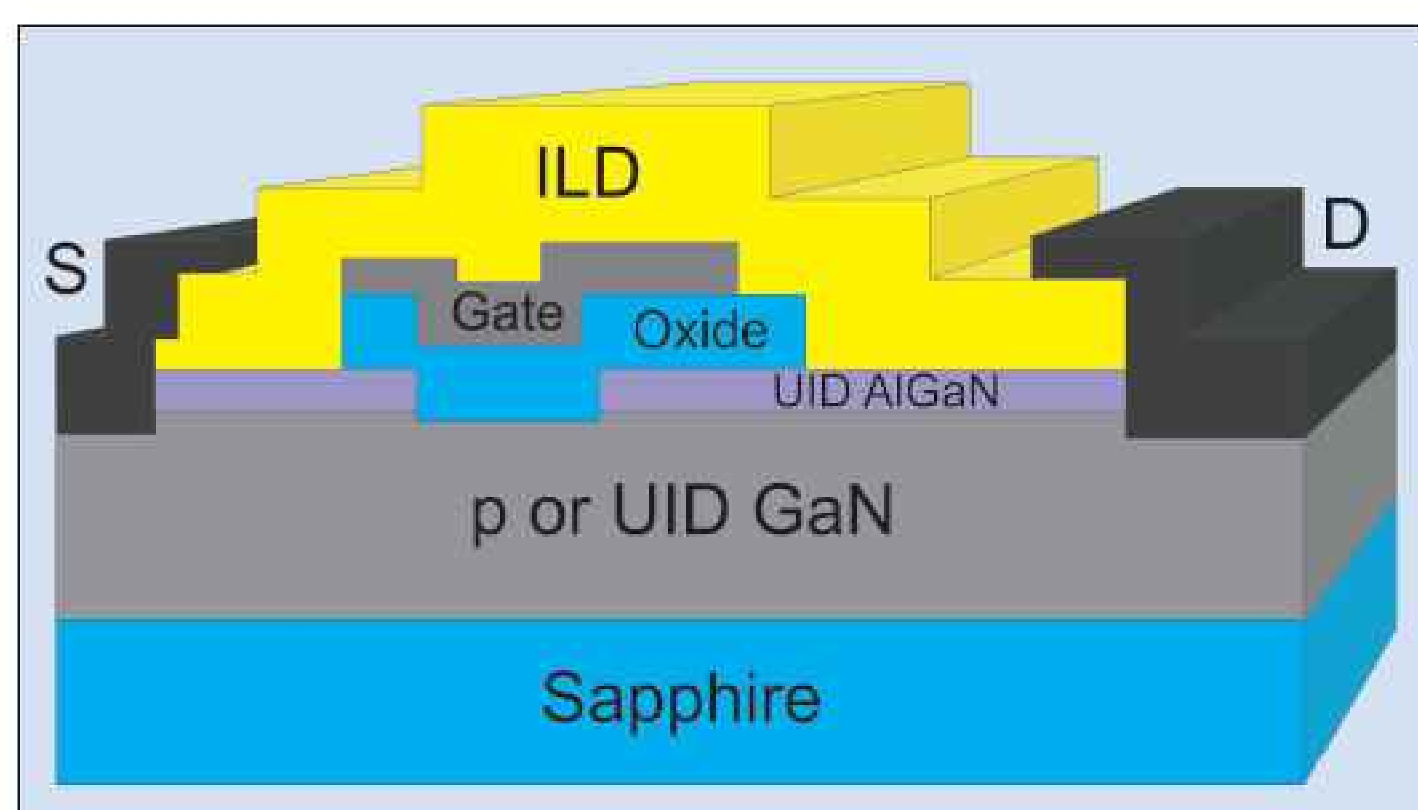

Figure 1. Schematic of hybrid MOS-HEMT device investigated in [2].

Further, polysilicon on silicon dioxide is an effective low-cost solution for gate electrodes.

Recently, there has been progress in developing suitable insulators for metal–insulator–semiconductor transistors based on III–V materials such as gallium arsenide, after some 20 years of stagnation in the area [1]. These renewed efforts have benefitted from the struggle of the mainstream silicon industry to move beyond the traditional SiO_2 gate insulation that is now becoming too thin for reliable devices. Different deposition techniques have been developed, with some coming from the compound semiconductor industry such as metal-organic chemical vapor deposition (MOCVD).

Among the groups researching oxides/insulators for III–V devices, a number have been developing materials for use in GaN gate stacks. For example, a group working under the direction of professor T Paul Chow at Rensselaer Polytechnic Institute (RPI) researches GaN MOSFETs using SiO_2 as the gate oxide, with one application target being power switching. The devices are made using standard tools from a silicon CMOS environment, says Chow. The GaN MOSFET process was developed by Chow's former PhD student Weixiao Huang. Chow sees such devices being used to implement

'smart power' in power supplies for low-voltage and battery-powered equipment. Chow has also worked on GaN MOSFETs with researchers at GE's Global Research center in New York State.

MOS-HEMT

At this May's International Symposium on Power Semiconductor Devices & ICs (ISPSD), an enhancement-mode hybrid MOS-HEMT built on GaN-on-sapphire was reported by a joint RPI/Furukawa Electric group [2]. The structure is designed to have a lightly doped drift region with a reduced surface field (RESURF) between the gate and drain to optimize the trade-off between the breakdown voltage and on-resistance of the device (Figure 1). An AlGaN/GaN heterostructure is incorporated into the RESURF region so that the drift occurs in a high-mobility two-dimensional electron gas (2DEG), while the current flow is controlled by a MOS gate stack. Using the AlGaN/GaN heterostructure instead of an ion implant to create the RESURF region avoids the need for extremely high-temperature annealing to activate the implant. The new arrangement results in a specific on-resistance as low as $20m\Omega/cm^2$ for a 20μm-long RESURF region.

First of all, the researchers carried out simulation work on the design concept to find appropriate parameters and dimensions for experimental devices. For example, the 2DEG carrier density was varied to find the maximum breakdown voltage. The model's optimum density for an unintentionally doped combination of AlGaN/GaN was found to be $5x10^{12}/cm^2$. However, this level creates too high a field in the oxide at the gate corners, making it difficult to create depletion and hence blocking current in the channel when the transistor is off. Balancing these contradictory needs limits the 2DEG carrier density to $2x10^{12}/cm^2$. A higher carrier density means lower resistance, and hence higher current flow. For a higher carrier concentration, a model with p-type GaN (with a doping concentration of $3x10^{16}/cm^3$) under the unintentionally doped AlGaN was considered. The 2DEG carrier density for maximum breakdown voltage was found to be $1.2x10^{13}/cm^2$. Taking into account the limitations from gate depletion, the 2DEG carrier density is found to be limited to $8x10^{12}/cm^2$ or less. Varying the p-type doping for the GaN layer was also considered, with a doping density of $2–3x10^{16}/cm^3$ found to be the best range in terms of long-term oxide reliability.

Actual devices were grown on 30nm of unintentionally doped $Al_{0.22}Ga_{0.78}N$ on a 3μm carbon-doped p-GaN buffer on sapphire. The general silicon dioxide insulation was 500nm thick, while the gate oxide was 100nm. The oxide was annealed at 900ºC for 30 minutes in an N_2 ambient. The temperature was lowered from the usual 1000ºC to protect the AlGaN/GaN heterostructure. Polysilicon was used for the gate electrode. The source/drain contacts were 20nm of titanium on

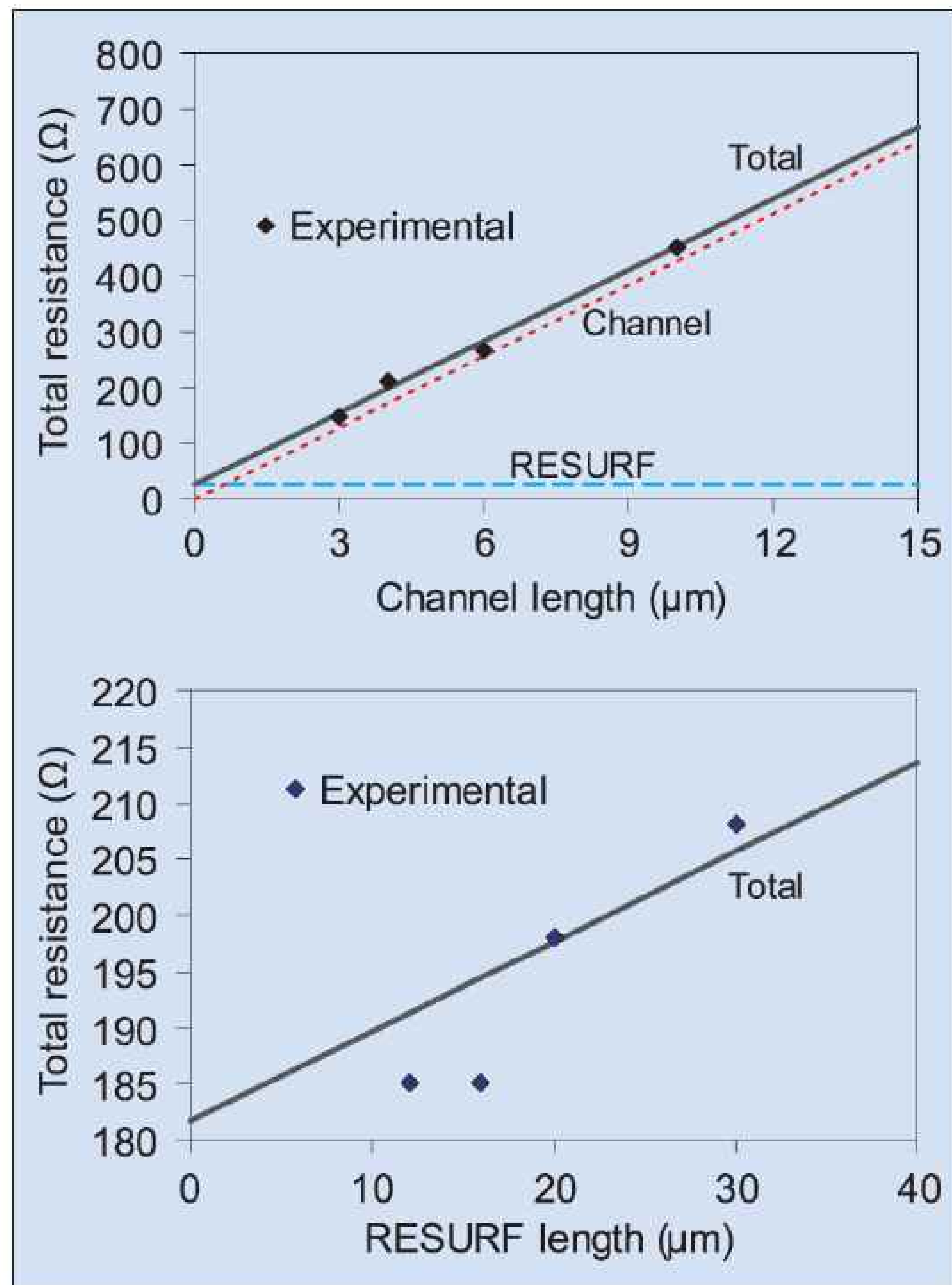

Figure 2. Experimental and model fit for on-resistance as function of channel and RESURF length for device in Figure 1.

300nm of aluminium. A Ti/Mo bilayer was used for the probe pads. Various RESURF region lengths were implemented in the range 8–30μm, with channel lengths of 2–10μm.

The model for the MOS-HEMT devices was tested by extracting parameters such as maximum field-effect mobility from circular GaN MOSFETs that were formed on the same wafer. The circular MOSFET devices were found to have a sub-threshold swing higher than previously obtained by the group. This poor performance was attributed to the wet etch step not completely removing damage from the more aggressive inductively coupled plasma (ICP) etch used to form the devices. CV measurements suggest that the lower anneal temperature also plays a role in the poorer performance. One result is that the maximum field-effect mobility of $79cm^2/V-s$ is about half the value for as-grown GaN MOSFETs.

With these values for the relevant parameters, it was found that the MOS-HEMT devices performed close to the model in terms of on-resistance dependence on channel and RESURF region lengths (Figure 2). A device with a 3μm channel, 20μm RESURF length and 600μm width was found to have a specific

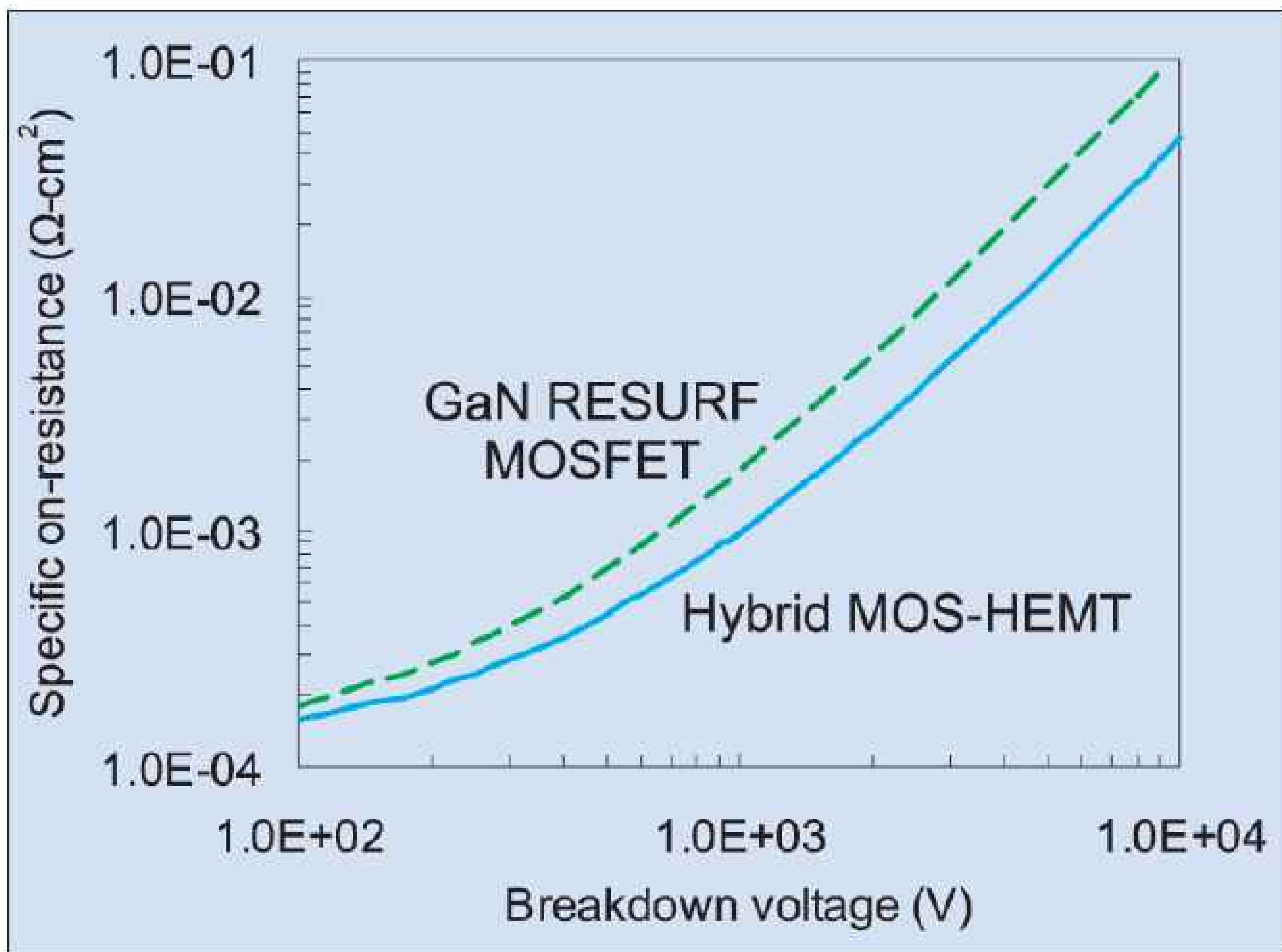

Figure 3. Specific on-resistance vs breakdown voltage for the device in Figure 1.

on-resistance of 20mΩ/cm^2 for a 30V gate voltage. For a 4μm channel and 20μm RESURF drift region, it is estimated that the channel contributes 84% of the resistance due to the poor mobility of p-GaN compared with the 2DEG in the drift region. The breakdown voltage of this device was 200V, which was attributed to oxide failure. However, it is thought that this can be improved by a better-quality p-GaN underlayer.

Using these results, it is found that the MOS-HEMT configuration has lower on-resistance over GaN RESURF MOSFET devices, both in devices with low breakdown voltage (BV) and even more so at higher BV ratings (Figure 3). For example, a 1200V MOS-HEMT device would have a specific on-resistance of 1.3mΩ-cm^2, a value that is 53% that of the equivalent MOSFET with just GaN in the RESURF region.

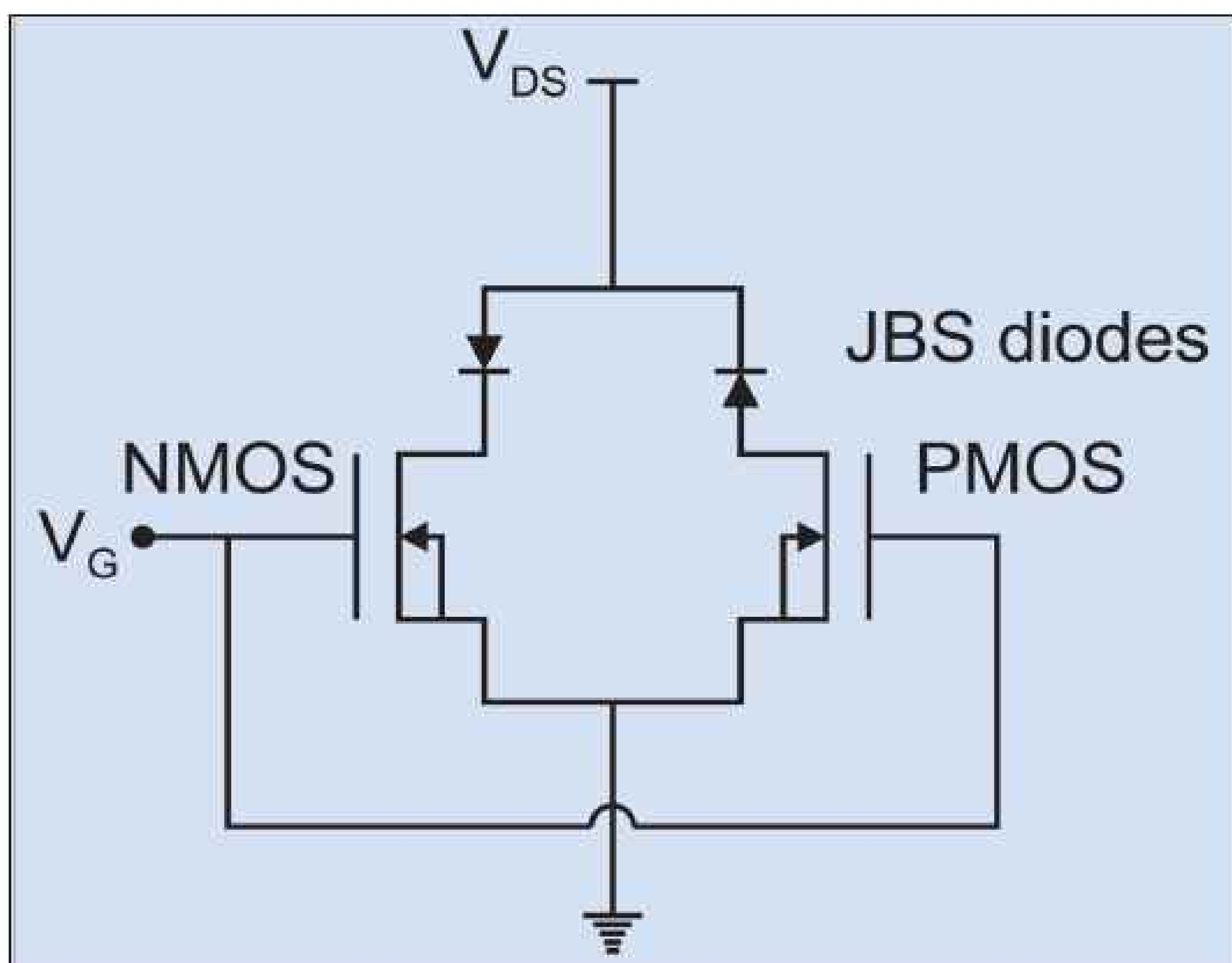

Figure 4. Bi-directional switch circuit structure.

GaN RESURF

Last year, a GaN RESURF region device was reported that integrated a MOSFET with an integrated Schottky diode [3]. The RESURF length dependence was studied up to 18μm. DC performance includes a blocking voltage of 770V in the forward direction and 1040V in the reverse direction. The device is designed to be half of a GaN bidirectional switch (Figure 4), realized as a pair of MOSFETs connected with a complementary pair of junction barrier Schottky diodes. In the half circuit, the current is blocked in the forward direction by the RESURF region and in the reverse direction by the Schottky diode (Figure 5). Again, simulations preceded the building of actual devices.

Devices were built on a 3μm unintentionally n-doped GaN epilayer on sapphire grown using MOCVD. Silicon ion implantation was used to create source/drain n doping. Annealing was carried out at 1100ºC to activate the silicon doping. Circular devices were created with a channel length of 4μm and a channel width of 800μm. The length of the RESURF drift region was varied between 6μm and 18μm.

From the experimental results, the forward voltage drop in the on state for a given breakdown voltage device was predicted to give an indication of the on-resistance. Beyond a breakdown voltage of 1000V the forward voltage drop rises rapidly from 1.2–1.3V, reaching ~10V at 10,000V (Figure 6). Beyond 5000V breakdown, bipolar structures would be needed to reduce on-resistance and hence bring power losses down to an acceptable level. Further problems would arise from integrating the p-channel half of the bi-directional switch due to the lower hole mobility in GaN.

Over a number of years, the RPI group [4] has reported on the properties of silicon dioxide deposition on GaN using different (and often unspecified) precursor recipes and process temperatures (300–900ºC).

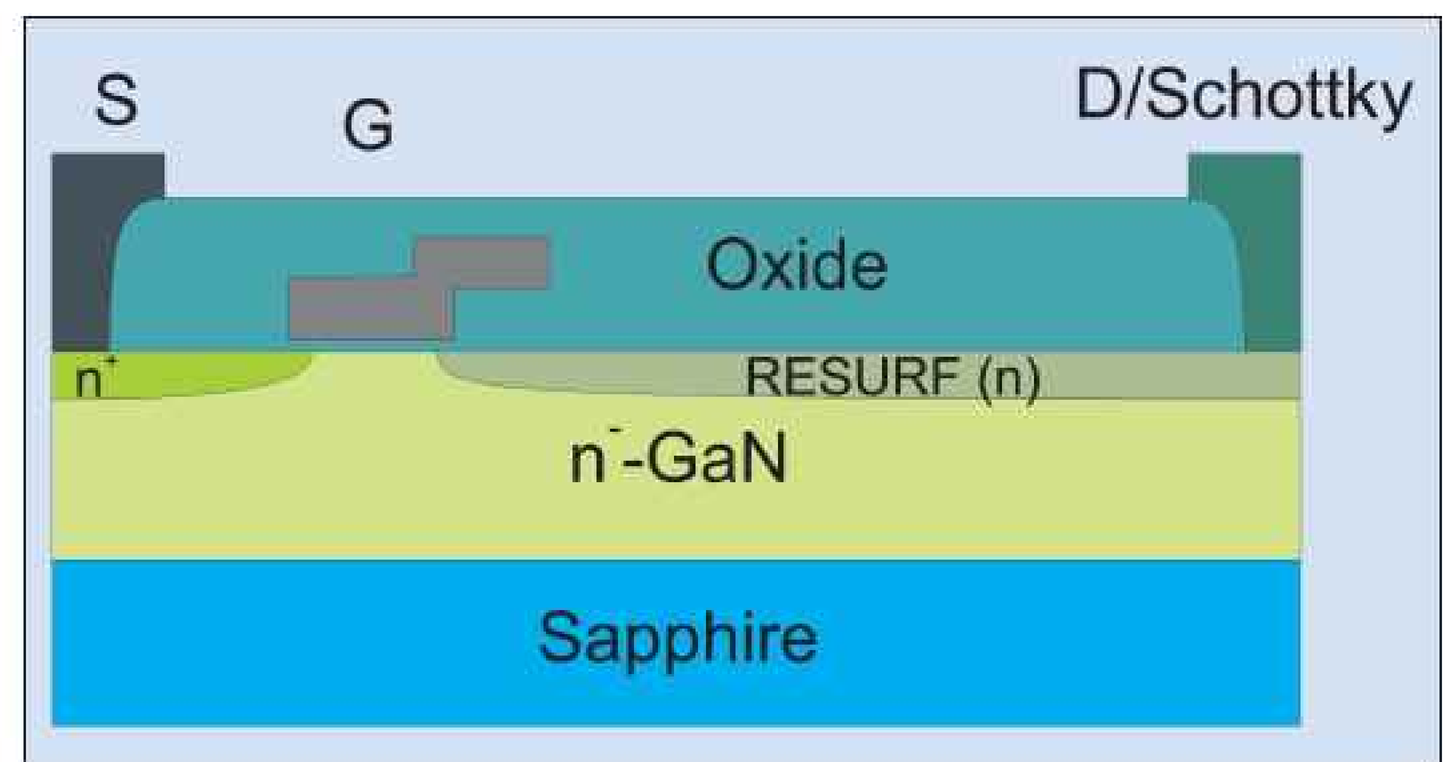

Figure 5. Schematic of half bidirectional switch of GaN MOSFET with integrated Schottky diode.

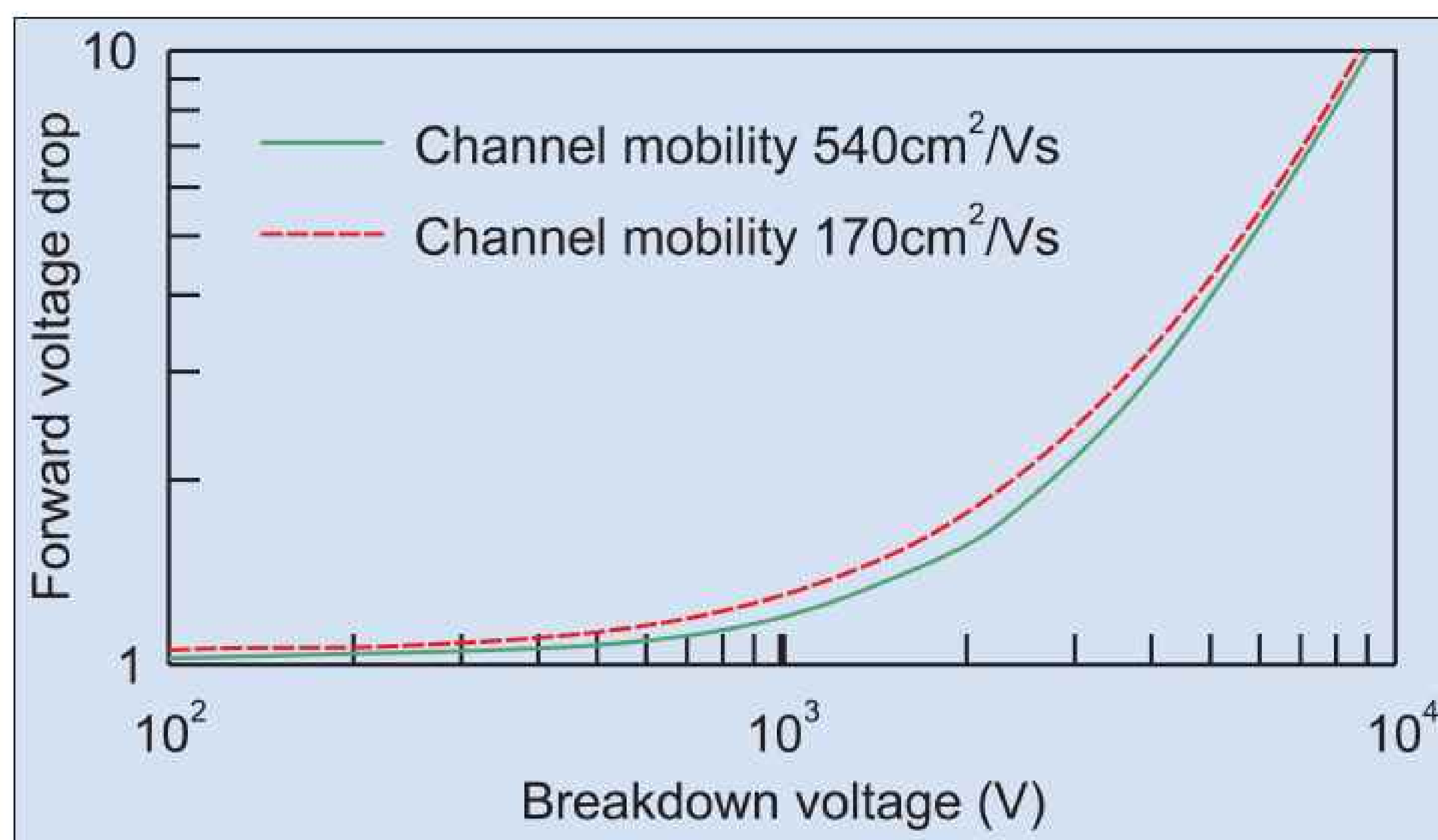

Figure 6. Predicted forward voltage drop for current density of 100A/cm^2 and given breakdown voltage for two channel mobilities and RESURF region mobility of 600cm^2/Vs. RPI achieved a mobility of 167cm^2/Vs.

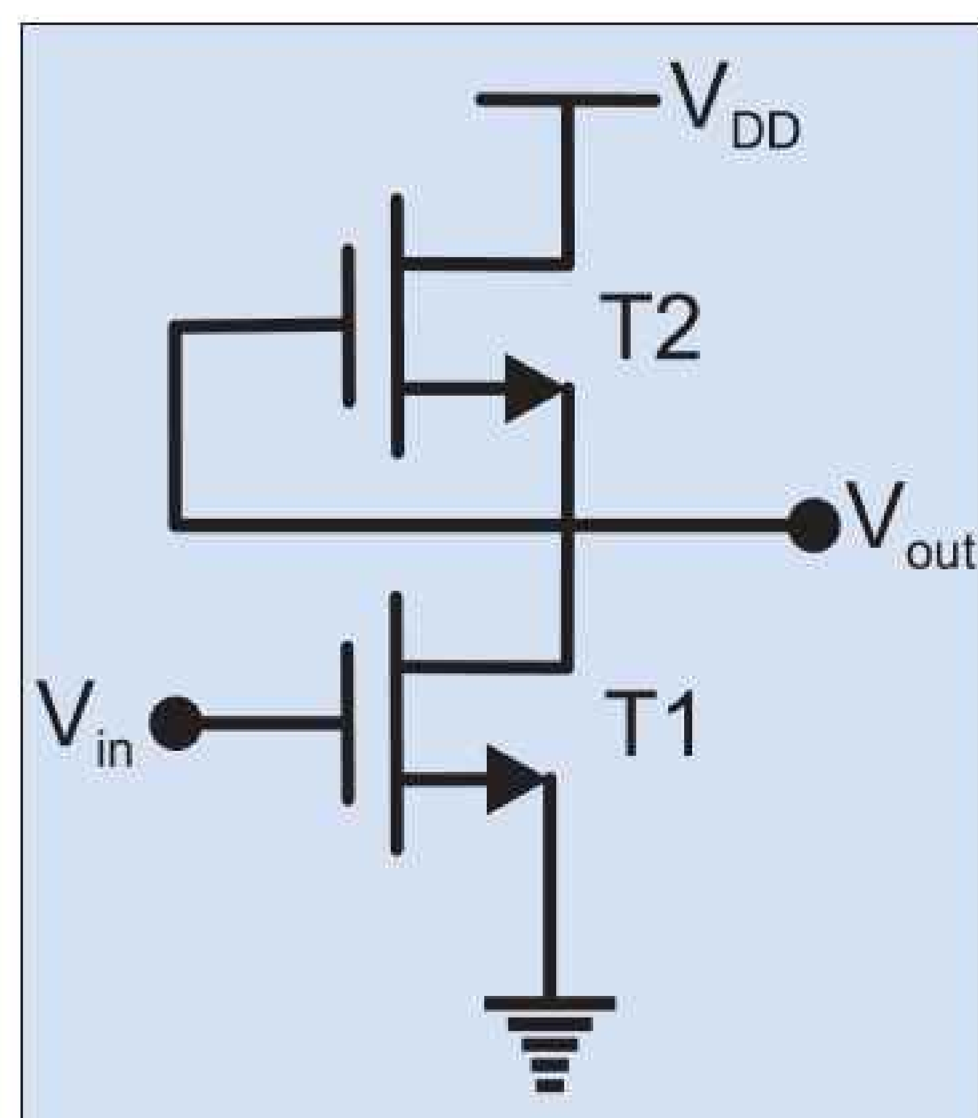

Figure 7. Schematic circuit diagram for a gallium nitride inverter device.

Measurements (CV, flat-band voltage shift) on GaN MOS capacitor formations to determine the levels of interface trap states and fixed charge in the oxide layer have resulted in one process (OX3 in [4]) that showed a low level of traps that decreases into the bandgap and a positive 1.5V flat-band voltage shift. Ultraviolet-induced flat-band voltage shift measurements on OX3 indicated a net interface charge of $1.6x10^{12}$q/cm^2 and fixed charge of $1.0x10^{12}$q/cm^2 (where q represents the elementary charge). The maximum field-effect mobility in circular MOSFETs was found to be 167cm^2/V-s, which is about 20% of the bulk value of ~900cm^2/V-s. However, even 20% was a world best for GaN MOSFETs, according to the researchers' knowledge.

A common problem in GaN HEMTs is the collapse of current at high source/drain voltages. Testing for current collapse in the GaN MOSFETs with pulsed gate voltages instead found increased currents. It is thought that the pulsed gate voltage creates less heating than a DC gate condition.

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An inverter circuit (Figure 7) built using the GaN MOSFETs showed good transfer characteristics.

The University of Florida has also been doing basic research on improved gate dielectrics for GaN MOSFETs over the past decade or so, under the direction of professors Steve Pearton and Fan Ren. Oxides with interface state densities as low as $1–3x10^{11}$cm^{-2} have been produced. Among the materials that were tried as an insulator on GaN at Florida (individually and in alloy form) are Ga_2O3, Gd_2O_3, Sc_2O_3, MgO, MgCaO, SiO_2, SiNx, and even low-temperature-deposited GaN.

Other work

Florida has used its GaN MOS technology to create MOS-HEMT hydrogen detectors. A variety of these devices have been deployed in the field for hydrogen sensing at a Ford dealership in Orlando, where a fleet of hydrogen-fueled cars are stored. Florida has also collaborated with researchers at Taiwan's National Cheng Kung (NCKU) and National Central (NCU) universities and at Toyota's central lab in Japan.

Florida, together with NCU and French epiwafer firm Picogiga International, has also investigated using GaN-on-silicon substrates to produce GaN MOSFETs [5]. GaN-on-silicon opens up possibilities of large-scale, low-cost production, perhaps even on the largest 300mm diameter wafers. Although silicon's lattice mismatch with GaN (~17%) is worse than sapphire's (~15%), the thermal conductivity of silicon is much better, which is an important consideration for power devices. Silicon carbide is another material that is used for GaN MOSFET growth — it has a much smaller lattice mismatch (~3%) and even better thermal conductivity than silicon. However, it is extremely expensive and is available only in diameters of up to 100mm.

The group at NCKU [6] has used SiO_2 to make a MOSFET with 13μm source-to-drain distance and a gate area of 8x40μm. The transconductance was 48mS/mm with a drain current of 250mA/mm at a 4V gate voltage. The gate voltage could also go up to 20V. More recently, an oxide layer containing Ga_2O_3 and Al_2O_3 was used to produce an AlGaN/GaN MOS-HEMT with a threshold voltage of –5V. The gate leakage was 50pA at a forward bias of 10V and 2pA at a reverse bias of –10V [Huang et al, IEEE Electron Device Letters, vol.29, p284, 2008]. A maximum transconductance of 50mS/mm was found at –2.09V.

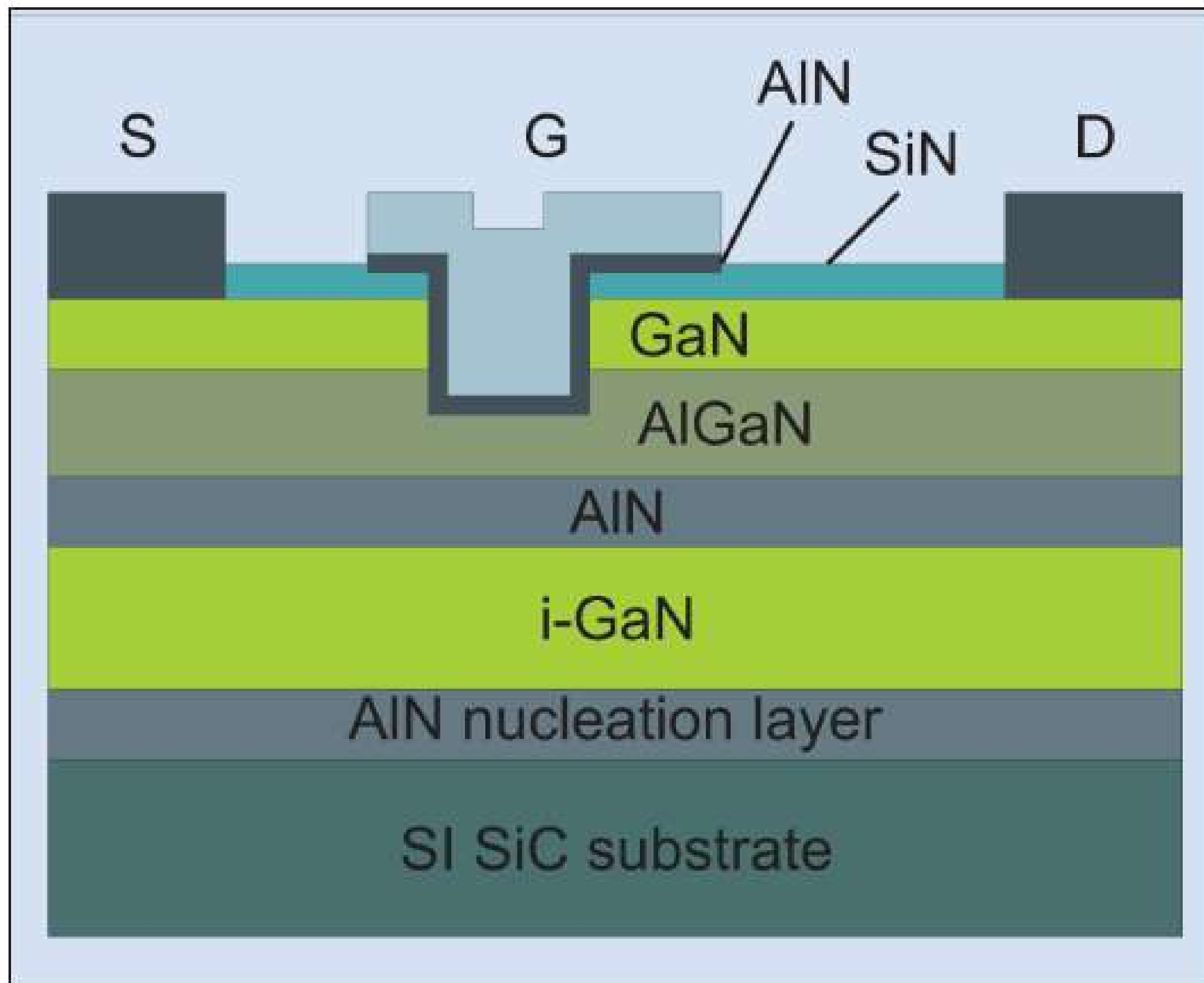

Figure 8. GaN MOSFET with AlN insulator on semi-insulating SiC substrate.

In 2000, researchers at China's Nanjing University [7] reported a GaN/AlGaN/GaN double-heterojunction structure with SiO_2 insulator and a gate that was 6mm long and 100mm wide. The DC transconductance was 0.6mS/mm and the maximum drain–source current was 5mA/mm. The gate leakage was less than 1μA at a bias of –10V and the gate breakdown was more than 20V. In 2006, the Nanjing team reported a 0.4μm AlGaN/GaN MIS-HEMT that used AlN as the insulator layer (Figure 8) [8]. The gate leakage at –80V was ~0.1mA/mm, which compares with a current in excess of 1mA/mm for a traditional Schottky gate GaN HEMT. The gate leakage also falls off faster for lower gate potentials.

A Yale University team [9] used jet vapor deposition (JVD) to investigate a $SiO_2/Si2N_3/SiO_2$ (ONO) stack in a MOS capacitor structure (i.e. without source and drain regions), which is often the first stage in demonstrating a gate stack for later use in a MOSFET structure. The gate leakage was described as 'very low', while interface traps and fixed oxide charge were 'low'. The hard-breakdown strength was 'extremely high'. ■

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